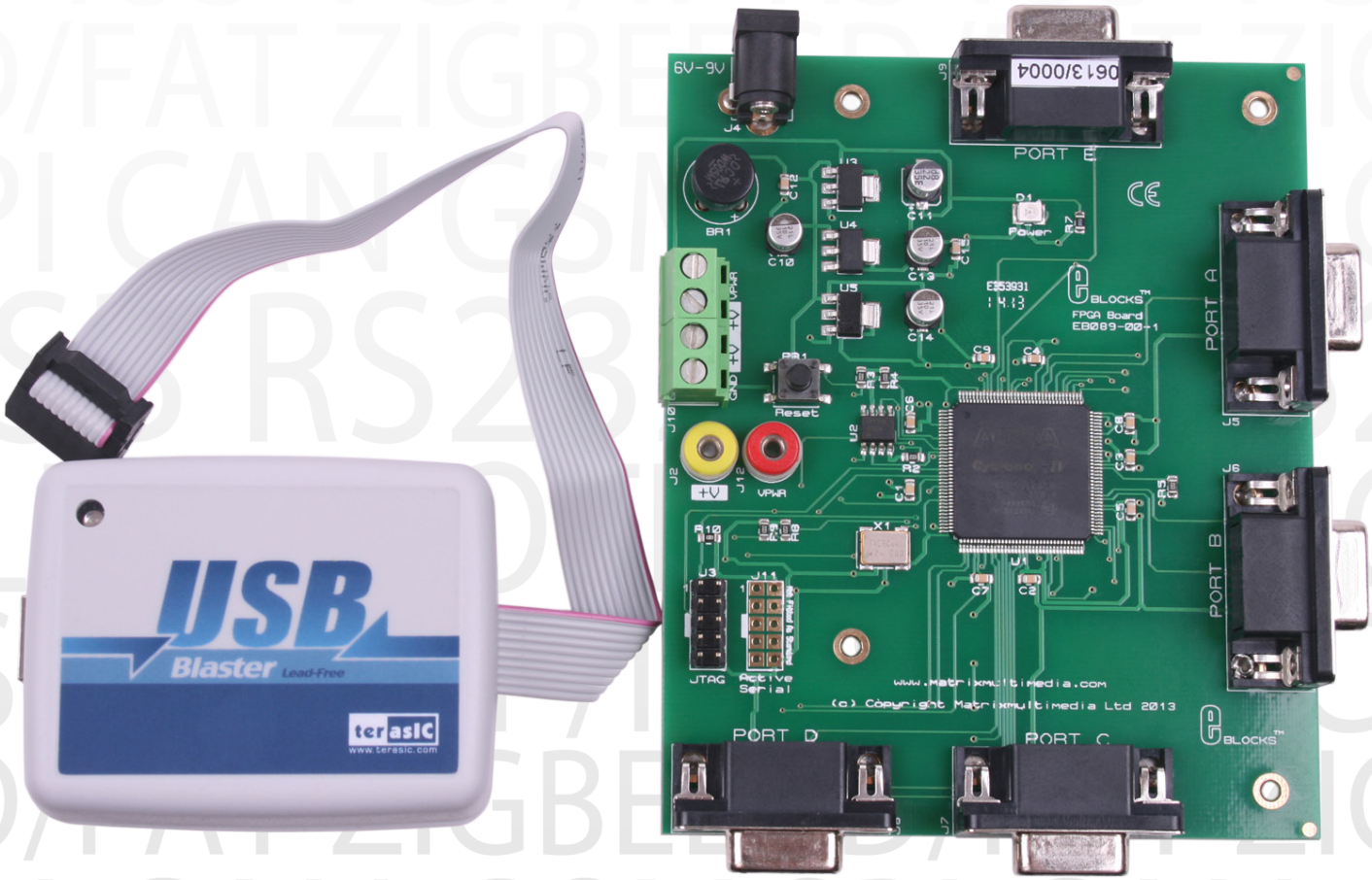
MATRIX

eBLOCKS®

FPGA Board



Contents

About This Document

This document concerns the E-blocks Cap Touch Keypad board with code EB089 version 1.

The order code for the FPGA board product is EB089.

1. Trademarks and copyright

PIC and PICmicro are registered trademarks of Arizona Microchip Inc. E-blocks is a trademark of Matrix Multimedia Ltd.

2. Disclaimer

The information provided within this document is correct at the time of going to press. Matrix Multimedia reserves the right to change specifications from time to time.

3. Testing this product

It is advisable to test the product upon receiving it to ensure it works correctly. Matrix provides test procedures for all E-blocks, which can be found in the Support section of the website.

4. Product support

If you require support for this product then please visit the Matrix website, which contains many learning resources for the E-blocks series. On our website you will find:

- How to get started with E-blocks - if you are new to E-blocks and wish to learn how to use them from the beginning there are resources available to help.
- Relevant software and hardware that allow you to use your E-blocks product better.
- Example files and programs.
- Ways to get technical support for your product, either via the forums or by contacting us directly.

General Information

1. Description

The FPGA Board connects to your PC via a Terasic USB Blaser which is then connected via a standard USB cable to provide you with a low cost FPGA development board and programmer which is both simple to setup and use. The board is fully compatible with a wide range of E-blocks which makes it an extremely flexible platform for learning and developing projects.

The FPGA Board allows in-circuit programming of an ALTERA® FPGA Cyclone IV device. This board is used together with Altera's free and comprehensive downloadable programming software, Quartus II. The board can be programmed using various programming techniques such as Schematic Entry, Block Diagram and Hardware Description Languages (HDLs such as AHDL, VHDL and Verilog). It provides 'clean' access to all available I/O lines on the relevant FPGA device.

Further information on E-blocks is available in a separate document entitled Introduction to E-blocks.doc.

2. Features

- E-blocks compatible
- Full suite of programming software
- 25MHz Xtal operation
- 5 full I/O ports

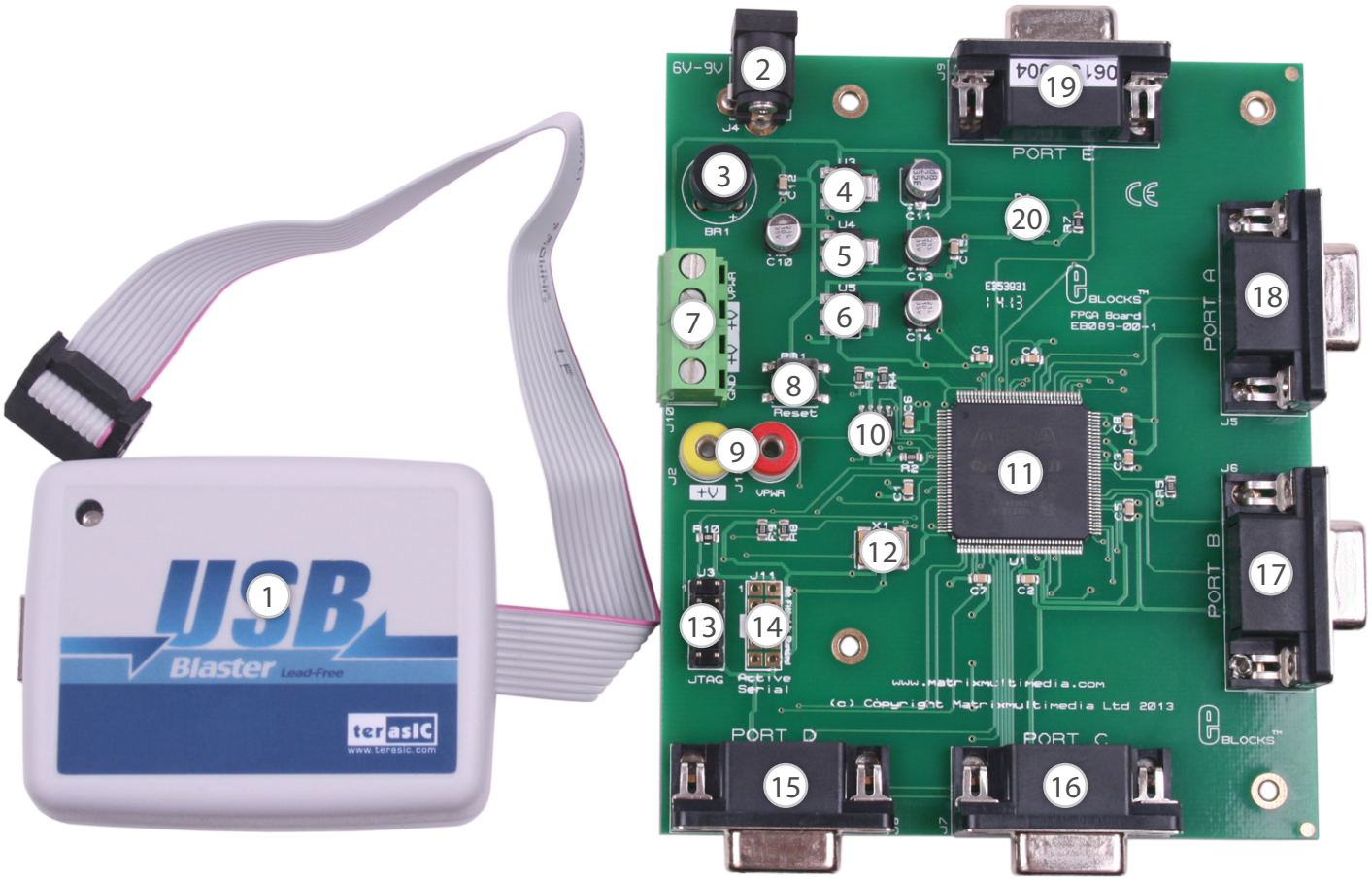
3. 3.3V operation

This board is fully compatible with 3.3V systems.

4. Block Diagram

A block diagram has not been provided for this board.

Board Layout



1) Terasic USB Blaster
2) PSU Connector 6-9V
3) Bridge Rectifier
4) Voltage Regulator VIO 3V3
5) Voltage Regulator VP 2V5
6) Voltage Regulator VCore 1V2
7) Power Screw Terminals
8) Reset Switch
9) 2mm Power Sockets
10) Altera Configuration Device
11) Altera FPGA Device
12) FPGA Crystal Oscillator
13) JTAG USB Blaster Header
14) Active Serial USB Blaster Header (not fitted a standard)
15) Port D
16) Port C
17) Port B
18) Port A
19) Port E
20) Power Status LED

Testing This Product

1. Installing Quartus II

The Quartus II software can be downloaded from Altera.com. You will need to sign up for an account before you can download and install the software.

2. Test Procedure

The following instructions explain the steps to test and use your FPGA Board. The instructions assume that Quartus II software is installed and functional. It also assumes that the test routine EB089_Test.jic file has been copied to a suitable place on your computer.

Follow these instructions to test the FPGA Board

1) Connect USB blaster to PC using USB cable and install the device driver from the "C:\Altera" folder.
2) Connect USB blaster to EB089 board ensuring notch on the cable matches the notch on the board.
3) Ensure power is supplied to the FPGA Board using a DC supply set to 6-9V.
4) Insert EB-004 LED board into any Port of the CPLD Board
5) Open Quartus II Web Edition
6) Launch the programming tool using the "Tools -> Programmer" menu.
7) Click "Hardware Setup"
8) Select USB blaster and then click close.
9) Click "Add File" button
10) Load the "EB089_Text.jic" file
11) Ensure the Program/Configure checkbox is ticked
12) Click the "Start" button.
13) When programming is complete press the reset button on the EB089 board.
14) Using the EB004 board test each of the EB089 ports and ensure every LED lights

This should satisfy that the FPGA Board is fully functional!

Circuit Description

The FPGA Board solution is made up of two parts: A circuit board that allows slave FPGA devices to be programmed, and the program to be executed 'seamlessly', and the Windows based programming utility Quartus II Web Edition.

1. Power Supply

The board can be powered from a 9V supply. The regulation circuitry will withstand unregulated 12V as a maximum input voltage and 6V as a minimum. If you are using a DC power supply then you should use a 7.5 or 9V setting. Power can be connected using the 2.1mm power jack or the screw terminal connectors J1, J2. The two "+V OUT" screw terminals are supplied for powering other E-blocks™, supplying approximately +3V3. LED D1 will indicate that power is connected to the board and that the voltage regulation circuitry is fully functional.
Please note connector J4 is directly connected to the J1 screw terminal pin 1 labeled VPWR, therefore any voltage input to J4 will also be available direct from pin 1 of J1.

Note: Remember that other E-blocks will have to receive +3V3 by placing a connecting wire from the "+V" screw terminal of the Multiprogrammer to the "+V" screw terminal of each E-Block that requires a voltage.

2. The FPGA

The FPGA that comes with this board is an 144-pin Altera® Cyclone IV series device, specifically the EP4CE10E22. The device has 10320 Macrocells available and 414Kb of Ram. This CPLD board utilizes 40 I/O pins, thus providing plenty of resources to set up both simple and complex projects.

3. I / O Ports

There are 40 dedicated I/O lines fed out to 5 D-type sockets grouped in ports, each port having 8 I/O lines. The pin-out of these ports can be found below

Note: All I/O available are clean signals – this means there is no protection. The user must be aware of this when selecting the functionality of the pins. Avoid connecting +V directly to an I/O pin or two outputs pins directly together – this can damage the FPGA device.

4. USB Blaster

The EB089 FPGA Board makes use of a USB blaster from Terasic to provide the programming functionality. This ensures for an easy setup on all computers and allows other Altera devices to be reprogrammed if required.

5. Port connections

The following table shows the pin connections on the 9-way D-type ports. This should be used for correctly setting the Pin location in the Quartus software.

PORT A D-type pin number	EP4CE10 pin number
1	B7_110
2	B7_111
3	B7_112
4	B7_113
5	B7_114
6	B7_115
7	B7_119
8	B7_120
9	GND

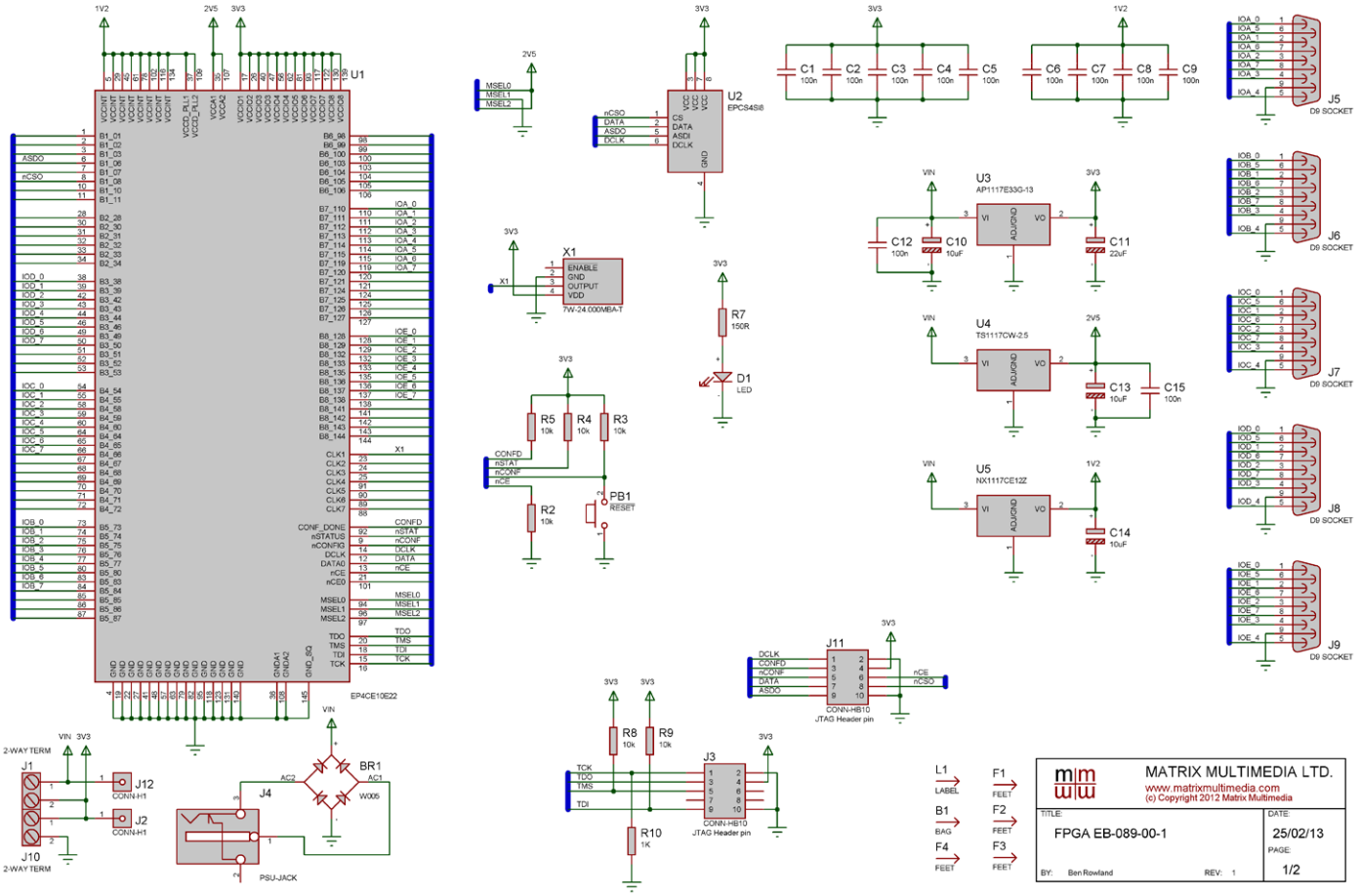
Port B D-type pin number	EP4CE10 pin number
1	B5_73
2	B5_74
3	B5_75
4	B5_76
5	B5_77
6	B5_80
7	B5_83
8	B5_84
9	GND

Port C D-type pin number	EP4CE10 pin number
1	B4_54
2	B4_55
3	B4_58
4	B4_59
5	B4_60
6	B4_64
7	B4_65
8	B4_66
9	GND

Port D D-type pin number	EP4CE10 pin number
1	B3_38
2	B3_39
3	B3_42
4	B3_43
5	B3_44
6	B3_46
7	B3_49
8	B3_50
9	GND

Port E D-type pin number	EP4CE10 pin number
1	B8_128
2	B8_129
3	B8_132
4	B8_133
5	B8_135
6	B8_136
7	B8_137
8	B8_138
9	GND

Circuit Diagram



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